Amendments to the Specification:

Page 4:

Please substitute the following paragraph for the paragraph beginning at line 17:

Fig. 9 is a ~~pan~~ plan view of an essential part of an instance of a wiring in an underlying layer of an electrode pad of a semiconductor device according to a further embodiment of the invention;

Page 14:

Please substitute the following paragraphs for the paragraphs beginning at page 14, line 5 through page 19, line 12:

Initially, an arrangement of the dummy wiring is illustrated. Figs. 1 to 3 are, respectively, a plan view showing an instance of an essential part of each of wirings MXa, MXb, MXc, MXd and MXe in a given wiring layer serving as an underlying layer of pads PD1 to PD3. Figs. 4 to 6 are, respectively, sectional views, taken along lines Y1-Y1, Y2-Y2 and Y3-Y3 at the wirings MXa to MXe of Figs. 1 to 3. The pads PD1 ~~t~~ to PD3 are, respectively, a portion at which a bump is bonded and are disposed at different positions of the active region of the same semiconductor chip. The pads

PD1 to PD3 are equal to one another with respect to the planar size and shape. The wirings MXa, MXb, MXc and MXd, respectively, indicate a wiring for signal or power supply which is necessary for constituting an integrated circuit of a semiconductor chip, whereas the wiring MXe indicates a dummy wiring not necessary for the arrangement of the integrated circuit of the semiconductor chip. All the wirings MXa to MXe are formed on an insulating film ISa by ~~pattering~~ patterning, for example, a metal film made mainly of aluminium or the like or a built-up conductor film ~~made a metal film~~ made mainly of aluminium or the like and other type of conductor film (e.g. a built-up conductor film obtained by depositing a metal film made mainly, for example, of titanium (Ti), titanium nitride (TiN), aluminium or the like and a film of titanium nitride in this order) according to photolithographic and etching techniques. Thee wirings are covered with an insulating film ISb. As is particularly shown in Figs. 3 and 6, the dummy wiring MXe is arranged in a region which corresponds to the pad PD3 region and in which any wiring would not be otherwise arranged. In this way, the occupation rate of the underlying wiring within the pad PD3 region is so designed as to be equal to the occupation rates of the underlying wirings within the pads PD1 and PD2 shown in Figs. 1 and 2. This permits the

upper levels of the ~~underlying~~ insulating film ISb within the regions of the pads PD1 to PD3 of Figs. 1 to 3 to be uniform as is particularly shown in Figs. 4 to 6. Moreover, the upper portions of the underlying insulating films ISb within the regions of the pads PD1 to PD3 can be improved with respect to the flatness thereof.

Although it is assumed that the dummy wiring MXe is provided as a wiring in a floating state which is not electrically connected with any other wiring, the dummy wiring may be formed by extending part of a wiring necessary for the arrangement of an integrated circuit (i.e. the wiring MXd in this case) to a region where the arrangement of a dummy wiring is required. In this case, although the wiring per se is not a dummy wiring, a wiring portion extending, for achieving the purpose of this embodiment, to a region not inherently required for arrangement of wiring is taken as a dummy. Figs. 7 and 8, respectively, show a modification of arrangement of dummy wiring. Fig. 7 is a plan view showing an instance of an essential part of a wiring formed at the same layer level as the wirings shown in Figs. 1 to 6, and Fig. 8 shows a sectional view taken along line Y4-Y4 at the wiring of Fig. 7. A pad PD4 indicates a pad which is located in an active region of the semiconductor chip different from the region where the pads

PD1 to PD3 of Figs. 1 to 3 are arranged, with its planar size and shape being same as those of the pads PD1 to PD3. Wirings MXf and MXg indicate wirings for signal or power supply which are necessary for the constitution of an integrated circuit of the semiconductor chip. Wiring MXh indicates a dummy wiring. In this connection, the occupation rates of the underlying wirings MXf and MXg within the region of the pad PDF are substantially same as those illustrated in Figs. 1 to 3. From the standpoint that the occupation rates are made uniform, any dummy wiring is not required, and such a dummy wiring is not arranged within a region of the pad PD4. In this case, the dummy wiring MXh is arranged in the vicinity of an outer periphery of the pad PD4. If this dummy wiring MXh is not provided, the insulating film ISb in the vicinity of the outer periphery of the pad PD4 is recessed at the upper surface thereof, thereby causing steps to occur. Because the flat area of a bump ~~boded~~ bonded with the pad PD4 is slightly larger than that of the pad PD4, the step at the upper surface of the insulating film ISb in the vicinity of the outer periphery of the pad PD4 is reflected on the upper surface of the bump electrode. As a result, the bump is impeded with flatness at the top thereof and may become, in some case, lower in height than the tops of other bumps. To avoid this, the

dummy wiring MXh is arranged in the vicinity of the outer periphery of the pad PD4, so that a step can be prevented from being formed at the upper surface of the insulating film ISb at the outer periphery of the pad PD4, thereby improving the flatness at the upper surface of the pad PD4 and thus ensuring the height of the pad PD4. In this way, the height at the top of the bump bonded with the pad PD4 can be mad equal to the height at the top of other ~~bump~~ bumps. It will be noted that the bumps are, respectively, formed in a uniform thickness. More particularly, a variation in thickness of bumps can be substantially neglected.

Next, how to arrange the above slits is illustrated. Figs. 9 to 11 are, respectively, a plan view showing instances of essential parts of wirings MXi, MXj, MXk and MXm in the same given wiring layer which is an underlying layer of the pads PD5 to PD7. Figs. 12 to 14 are, respectively, sectional views, taken along lines Y5-Y5, Y6-Y6 and Y7-7 at the wirings MXi, MXj, MXk and MXm of Figs. 9 to 11. The pads PD5 to PD7 are similar to the pads PD1 to PD3, and are not particularly illustrated. The wirings MXi, MXj, MXk and MXm, respectively, indicate those wirings for signal or power supply necessary for arrangement of an integrated circuit of a semiconductor chip. The materials

and forming method of these wirings MXi, MXj, MXk and MXm are similar to those of the wirings MXa and the like. As is particularly shown in Figs. 10, 11, 13 and 14, a slit SL is formed in part of the wirings MXk and MXm, respectively. The slit or slits SL are formed by removing part of the wiring MXk and MXm. This permits the occupation rates of the underlying wirings within the pads PD6, PD7 to become equal to the occupation rate of the underlying wiring within the pad PD5 of Fig. 9. In this manner, the heights of the upper surfaces of the underlying insulating film ISb within the regions of the pad PD5 to PD7 can be made uniform as shown in Figs. 12 to 14. In addition, the flatness at the upper portion of the underlying insulating film ISb within the pad PD5 to PD7 can be improved. The slit SL may be formed at the center of the wiring MXk as shown in Fig.10, or may be formed as extending from the outer periphery of the wiring MXm toward the center as shown in Fig. 11. In this embodiment, the ~~slid~~ slit SL of Figs. 10 and 11 is formed at a position of the space between adjacent wirings MXi and MXj of Fig. 9. This allows the underlying states of the pads PD5 to PD7 to become more uniform, thereby ensuring a more uniform height and more improved flatness at the upper surface of the underlying insulating film ISb within the regions of the pads PD5 to PD7.

Page 25:

Please substitute the following paragraph for the paragraph beginning at page 25, line 20 through page 26, line 20:

Next, a specific application of the semiconductor device according to this embodiment is described. Fig. 25 is a plan view showing, as a whole, an instance of a semiconductor chip 1C for constituting the semiconductor device of this embodiment. This semiconductor chip 1C has, for example, a substrate 1S which is formed in an elongated, rectangular shape and also has, on a main surface thereof, a LCD drive circuit for driving a liquid crystal display (LCD). This LCD driver circuit has the function of supplying a voltage to individual pixels of a cell array of LCD to control the direction of liquid crystal molecules, and has a gate drive circuit 3, a source drive circuit 4, a liquid crystal drive circuit 5, a graphic RAM (random access memory) 6 and a peripheral circuit 7. In the vicinity of the outer periphery of the semiconductor chip 1C, there are arranged the plural pads PD at given intervals along the outer periphery of the semiconductor chips 1C. These plural pads PD are provided on the active region where elements and wirings of the semiconductor chips are arranged. These

plural pads PD includes pads for integrated circuit necessary for constituting an integrated circuit and dummy pads not necessary for the constituting an integrated circuit. The pads PD are arranged in a zigzag form in the vicinity of one long side and two short of the semiconductor chip 1C. The plural pads arranged in the zigzag form are made mainly of those for gate output signal and source output signal. More particularly, the plural pads, which have been arranged in a zigzag form at the center of the long side of the semiconductor chip 1C are for source output signal, and the plural ~~pad~~ pads, which have been arranged in a zigzag form along both short sides of the semiconductor chip 1C are for gate output signal. Such a zigzag arrangement permits a large number of pads required for gate and source output signals to be arranged while suppressing the semiconductor chip 1C from increasing in size. More particularly, the chip size can be reduced, and the number of pads (pins) can be increased. A plurality of pads PD arranged in parallel to one another, not in a zigzag form, in the vicinity of the other long side of the semiconductor chip 1C are those pads for digital or analog input signal. In the vicinity of the four corners of the semiconductor chip 1C, pads PD having a relatively large planar size are arranged. This relatively large-sized PD pad indicates a

corner dummy pad. The relative small pad PD has a planar size, for example, of about 35 μm x 50 μm. The planar size of the relatively large-sized pad PD (corner dummy pad) is, for example, at about 80 μm x 80 μm. The pitch of the adjacent pitch is, for example, at about 30 μm to 50 μm. The total number of the pads PD is, for example, at about 800.

Page 38:

Please substitute the following paragraph for the paragraph beginning at page 38, line 2 through page 41, line 11:

Next, an example of a manufacturing procedure of the semiconductor device illustrated hereinabove is described. The isolation portion 2 is formed in the main surface of the substrate 1S constituting a wafer which is substantially circular in plane, for example, by a LOCOS technique, thereby forming the active regions La, Lb. Thereafter, an element is formed in the active region La surrounded by the isolation portion 2. No element is formed in the active region Lb below the dummy pad PD16. Subsequently, the insulating film IS1 is deposited over the main surface of the substrate 1S by a CVD (chemical vapor deposition) method, followed by forming contact holes CNT of a circular

form in plane at given portions of the insulating film IS1 according to photolithographic and dry etching techniques. Thereafter, a titanium nitride film, a titanium film, an aluminium film and a titanium nitride film are, for example, deposited on the insulating film IS1 in this order by a sputtering method or the like. The thus deposited metal film is subjected to patterning by photolithographic and dry etching techniques to form the first-layer wiring M1. Next, the insulating film IS2 is deposited on the insulating film IS1 in a similar way, and the through-holes TH1 are formed in the insulating film IS2, followed by forming the second-layer wiring M2 on the insulating film IS2, like the first-layer insulating M1. The insulating film IS3 is likewise deposited over the insulating film IS2 and the through-holes TH2 are formed in the insulating film IS3, followed by forming the third-layer wiring M3 on the insulating film IS3, like the first-layer wiring M1. In order that the occupation rates of the respective wirings are made uniform as stated hereinbefore, these wiring layers are appropriately provided with the slits SL (not shown). For instance, after formation of the ~~fist~~ first-wiring layer M1, grooves are formed in the first wiring layer M1 by patterning with photolithographic and dry etching techniques. Thereafter, the insulating film IS2 is buried in

the grooves by the step of depositing the insulting film IS2 to form the slits SL. In case where the slit SL is, respectively, formed in other wiring layers including the second wiring layer M2 and the third wiring layer M3, a similar procedure can be used. Thereafter, after deposition of the insulating film IS4 for surface protection on the insulating film IS3, the opening 9 is formed in the insulating film IS4 so that part of the third-layer wiring is exposed, thereby forming the pad PD. Next, a single film of a high melting metal film such as, for example, titanium, titanium tungsten or the like, or a conductive film of a built-up film having structure wherein a nickel film and a gold film are built up on a titanium film in this order is deposited by a sputtering method or the like, followed by forming a photoresist pattern in such a way as to expose a bump-forming region and cover the other regions therewith. The bump 11 made, for example, of gold is formed by plating or the like, followed by removing the photoresist pattern and further the underlying conductive film by etching, thereby forming the underlying metal film 10. In this manner, a semiconductor device having the bumps 11 on the respective pads is fabricated. In the course of such fabrication of the semiconductor device, the upper surfaces of the insulating films IS1 to IS3 are flattened according

to an etch back method for a chemical mechanical polishing (CMP) method, thereby permitting the upper surface levels of a plurality of pads Pd within the main surface of the semiconductor chip 1C, i.e. the top levels of the bumps, to be made more uniform. Additionally, the flatness at the upper surfaces of the respective pads PD can be improved. In case where the etch back method is adopted, for example, the insulating film IS1 is deposited and its upper surface is etched back. Thereafter, the insulating film IS2 is deposited thereon, with its upper surface being further etched back. In this way, it is preferred that etching back is performed on each of the insulating films IS1 to IS3 by an anisotropic dry etching technique. On the other hand, where the CMP method is adopted, good results are obtained by performing CMP only on the upper surface of the underlying insulating film IS3 alone where the pad PD is formed, although each of the insulating films IS1 to IS3 may be subjected to CMP. More particularly, the uniformity of the height or level at the top of the bumps 11 can be enhanced by subjecting the respective insulating films IS1 to IS3 to etching-back or CMP, or by subjecting the insulating film IS3 alone to CMP at the upper surface thereof.

Page 43:

Please substitute the following paragraph for the paragraph beginning at page 43, line 15 through page 46, line 1:

Next, an instance of LCD assembling the semiconductor device of the embodiment is described. Fig. 49 is a plan view of an essential part of LCD 14, Fig. 50 is a sectional view of the essential part of Fig. 49, Fig. 51 is an enlarged, sectional view of the essential Part of Fig. 50, and Fig. 52 is an enlarged, sectional view of Fig. 51. LCD 15 has a liquid crystal panel, a semiconductor chip 1C for LCD drive, and a back light. The liquid crystal panel 16 has two glass substrates 16a, 16b of a rectangular form in plane, a seal member 16c provided between the two glass substrates 16a, 16b at the peripheral portions thereof, a liquid crystal material 16d sealed between the two glass substrates 16a, 16b, and a polarizer plate ~~attacked~~ attached at the back side of the front surface of the liquid crystal panel 16. LCD 15 includes an active type using a thin film transistor (TFT) and a passive type using a simple matrix liquid crystal (super twisted nematic). With the active type, an array of pixels which indicate a minimum unit for displaying a letter or picture on a screen, and wirings 17, such as a gate wiring and a source wiring, for driving the

pixels are formed. In this case, each of a plurality of pixels has TFT and a capacitor. With the active type, a color filter is formed at the glass substrate 16b. In this case, alkali-free glass is used, for example, as a material of the glass substrates 16a, 16b. On the other hand, with passive type, the glass substrates 16a, 16b are, respectively, formed thereon with wirings 17 extending along mutually intersecting directions. A phase difference plate is provides, aside from the polarizer plate. In this case, soda lime or low alkali glass is used, for example, as a material for the glass substrates 16a, 16b. With either the active type or the passive type, a transparent conductive film (ITO: indium tin oxide film) made of indium and tin oxides is used, for example, as the wiring 17. In either case, the semiconductor chip 1C is connected to the glass substrate 16a, for example, through an anisotropic conductive film (ACF) 18 in such a state that the surface (i.e. the surface on which the wirings 17 are formed) on which the bumps 11 are formed is directed toward the main surface of the glass substrate 16a (i.e. COG: chip on glass). The anisotropic conductive film 18 is made of an electric connection material, which is made, for example, by dispersing or orienting conductive particles 18b, such as carbon black, nickel fine particles or ball solder, in an

insulating bonding agent made of a thermosetting resin such as an epoxy resin. The bumps 11 of the semiconductor chip 1C and the wirings 17 of the glass substrate 16a are electrically connected with one another by means of the conductive particles 18b interposed therebetween in a crushed condition. An anisotropic conductive paste (ACP) may be used in place of the ACF. The wirings at the outer periphery of the glass substrate 16a is electrically connected with a printed board 20 through a flexible substrate 19. The flexible substrate 19 includes a substrate body 19a made, for example, of a polyimide ~~rein~~ resin or the like and a wiring 19b bonded to the surface of the body and mainly composed of copper (Cu). The wiring 19b of the flexible substrate 19 is electrically connected to the wiring 17 of the glass substrate 16a at one end thereof through the anisotropic conductive film 18 in the same manner as with the semiconductor chip 1C. On the other hand, the other end of the wiring 19b is electrically connected to the wiring of the printed board 20 by means of a solder 21 or the like. The printed board 20 mounts thereon a semiconductor chip for control circuit for controlling the operation of a LCD driver circuit of the semiconductor chip 1C, or the like electronic parts.